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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/926,202	09/24/2001	Hiroshi Takeno	P107242-00024	6219

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EXAMINER	
RAO, G NAGESH	
ART UNIT	**PAPER NUMBER**
1722	

DATE MAILED: 09/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/926,202	TAKENO, HIROSHI	
	Examiner	Art Unit	
	G. Nagesh Rao	1722	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-9 and 14-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-9 and 14-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1) Claims 6-9 and 14-17 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Miyashita 5,951,755.

Miyashita 755 pertains to a manufacturing method of semiconductor substrates, whereby its principle embodiment is the process for making a silicon

epitaxial wafer comprising the following steps below. Examiner wishes to note, that Miyashita 755 teaches a variety of preferred embodiments all of which can be interchangeable with one another.

Miyashita 755 teaches forming an epitaxial layer on a silicon substrate with an interstitial oxygen concentration range of 1.0×10^{18} atoms/cm^3 at a temperature of approximately 1000 ^{0}C whereby following with a low temperature annealing between the range of 400-800 ^{0}C. Lastly the epitaxial wafer substrate has a specific resistance (synonym of resistivity) of .008 Ω-cm and is doped with a concentration of Boron (Col 5 Lines 11-27).

Now Examiner has noted in the aforementioned a process that has met all the limitations required for applicant's claims, except for the interstitial oxygen concentration limitation. However examiner has noted that Miyashita 755 teaches the above process as a base of set parameters for creating the silicon epitaxial wafer and that alternative embodiments do exist. As noted in Miyashita 755's fourth embodiment, Miyashita 755 teaches the wafer having a 8×10^{17} atoms/cm^3 concentration of interstitial oxygen in the silicon epitaxial wafer. This range falls within the claimed oxygen concentration range as claimed by applicant (See Col 8 Lines 26-30 for an example). This being the case renders the oxygen concentration

to be easily modified and the process as claimed by applicant to be obvious as a result of routine experimentation.

Therefore it is the examiner's position that Miyashita 755 has met the criteria for rejection via a 102/103 rejection.

Claim Rejections - 35 USC § 103

2) The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3) Claims 6-9 and 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wijaranakula (5,611,855) in view of Wolf et al. (Silicon Processing for the VLSI Era Volume 1: Process Technology, Lattice Press, Sunset Beach, CA, USA, pp. 26-30, 59-61, 124, 133-136).

Wijaranakula 855 discloses a method of making an epitaxial Si wafer with certain properties. The process is disclosed in col. 4 lines 15+. A doped (with boron, arsenic, antimony) Si substrate with a dissolved oxygen concentration of between 10-50 ppma (parts per million atoms) is used. Col. 5 lines 1-67 details the

growth of an epitaxial layer on the wafer. The Si epitaxial wafer is annealed at between 600'C and 900'C to form oxygen microdefects in the wafer.

Wijaranakula 855 does not disclose the deposition temperature of the epitaxial layer, the oxygen concentration in units of atoms/cm^3, or the substrate's resistivity.

Wolf et al. discloses known Si physical properties. On page 59, the typical concentration of oxygen in Si is given as $5x10^{17}$ to $1x10^{18}$ atoms/cm^3 or 10-20 ppma. On page 135 it is disclosed than Si epitaxial growth is favored over etching in the range of temperatures from 900'C to 1400'C. Temperature optimization for annealing is disclosed on pages 60-61 and annealing from 650' to 750' C is discussed. On page 27 it is disclosed that Si doped with boron and antimony can have resistivities of from 0.005 ohm-cm upwards. Wolf et al. discloses the use of oxygen precipitates and denuded zones as gettering on page 61.

It would have been obvious to one of ordinary skill in the art at the time of the present invention to combine Wijaranakula 855 with Wolf et al. because Wolf discloses temperatures for epitaxial growth and annealing, a basis for comparing oxygen concentrations quoted in different units, resistivity of boron and antimony doped Si, and the known useful gettering action of oxygen precipitates in Si wafers.

It would have been obvious to one of ordinary skill in the art at the time of the present invention to form a Si epitaxial wafer doped with boron (or antimony or arsenic) at a temperature of 1000'C or higher on a Si substrate having a oxygen concentration of $4x10^{17}$ to $10x10^{17}$ (equivalent to $1x10^{18}$)/cm3 and then heat treating the wafer at a temperature of from 450'C to 750'C because such is suggested by Wijaranakula 855 in light of Wolf et al.

It would have been obvious to one of ordinary skill in the art at the time of the present invention that the resistivity of such a wafer would include the range of 0.02 ohm-cm or lower because such is disclosed by Wolf et al. for doped Si wafers and such resistivity was disclosed by Wolf et al. on page 26 as known to be a function of doping concentration.

It would have been obvious to one of ordinary skill in the art at the time of the present invention to optimize the process parameters including temperature such that oxygen precipitation nuclei were formed (thus increasing the bulk defect density) and not reducing the needed and well known use of the bulk Si oxygen precipitates for gettering purposes because Wolf et al. discloses such use for oxygen precipitates in the bulk of Si wafers and temperatures for annealing such wafers.

Response to Arguments

4) Applicant's arguments filed 8/25/06 have been fully considered but they are not persuasive.

In response to the argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). The examiner has shown that the ranges and known results of the use of those ranges in oxygen precipitate gettered Si-epitaxial wafers typical in the art suggest the claimed Si epitaxial wafer.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The combined references described previously by the examiner suggest a silicon wafer with a grown epitaxial Si layer thereon which is

subsequently annealed to produce oxygen precipitates (bulk defects therein) which were known to act as gettering sites. The oxygen concentrations and the temperatures claimed were within the known ranges described by the references. One of ordinary skill in the art would have expected gettering to occur in Si-epitaxial wafers grown under these conditions.

The claim that the gettering effect with a doped Si wafer is not suggested by the references is not persuasive. Wijaranakula 855 discloses using a boron (i.e. a P-type) ,phosphorous (N-type), or non-doped (I-type) wafer in col. 4 lines 15-25. This, combined with Wolf et al. suggests the claimed gettered epitaxial –Si wafer manufacturing process.

Lastly Examiner wishes to note that newly applied reference Miyashita 755 further shows that the claimed invention has already been known and disclosed, further substantiating on the combined teachings of Wijaranakula 855 and Wolf as not being improper but obvious to one having ordinary skill in the art at the time of the invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to G. Nagesh Rao whose telephone number is (571) 272-2946. The examiner can normally be reached on 9AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Yogendra Gupta can be reached on (571)272-1316. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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